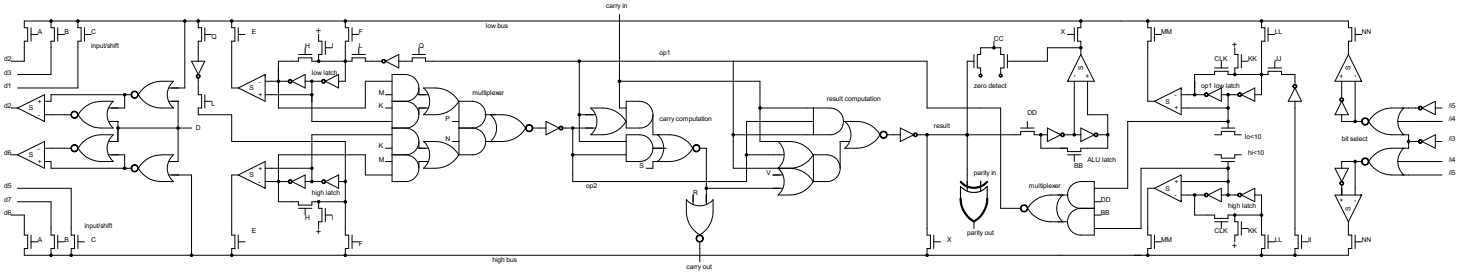
carry in
low bus
op1
op2
high bus
carry out
input/shift
low latch
high latch
multiplexer
carry computation
result computation
result
zero detect
parity in
parity out
ALU latch
op1 low latch
op1 high latch
bit select
lo<10
hi<10
d2
d3
d1
d5
d7
d6
i5
i4
i3
i4
i5